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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,057	12/04/2003	Hajime Kimura	12732-186001 / US6794	8774

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EXAMINER	
NGUYEN, KHAI M	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,057	KIMURA, HAJIME	
	Examiner	Art Unit	
	Khai M. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15,16,25,27 and 29* is/are allowed.

6)☒ Claim(s) *1-14,17-24,26,28 and 30-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-14, 17, 19-21, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsusaka (US 6,498,575 B2).

Regarding claims 1, 3-4, & 30, Matsusaka discloses a semiconductor device (Figs. 1-2) comprising: several pieces (k pieces – column 7, lines 42-52) of current sources; and a switching circuit (comprising of k pieces of sub-switching circuit 504 – column 7, lines 54-64) including: a plurality of input terminals (2 * k inputs, wherein k is the numbers of the circuits 504 or current sources 503) (see Fig. 2 for an example of the switching circuit 504 shown in Fig. 1); and a plurality of output terminals (75-76 of Fig. 2) wherein the current sources (k x I currents) and the output terminals of the switching circuit are electrically connected to each other (according to selection signals, SEL1 & SEL2, as seen in Figs. 1-2), and the switching circuit (504s) selects the output terminals (75-76) to be connected to the input terminals (71-72) by using signals (provided from the decoder circuit 501) which are input to the input terminals of the switching circuit.

Regarding claim 2, Matsusaka discloses the switching circuit (504s) of claim 1 which is controlled, in addition to the selection signals, by external/bias signals (78 of Fig. 5, 77 of Fig. 7, and 79-80 of Fig. 8).

Regarding claims 5-6, 22-23, & 31-32, Matsusaka discloses a device (see the drawings above), including: a plurality of current sources (k x I currents); and a switching circuit (that is the switching circuits 504) including n-pieces of input terminals (71-72; Fig.2) and m-pieces of output terminals (75-76; Fig. 2), wherein the current sources are each connected to one of the different output terminals (75s or 76s of Figs. 1 & 2), at least one of the input terminals of the switching circuit is connected to one or a plurality of switches (when one of the transistors 73 or 74 is ON), the switch is connected to one of the m-pieces of the output terminals (75-76), and the switching circuit (504) controls ON/OFF of the switch (the transistor 73 and/or 74) by using a signal(s) (either SEL1 or SEL2) which is input from at least one of the n-pieces of the input terminals (71-72).

Regarding claims 7 and 20, Matsusaka discloses the switching circuit (of claim 5) controls ON/OFF of the switching circuit by further using a signal, which is input externally (78 of Fig. 5, 77 of Fig. 7, and 79-80 of Fig. 8).

Regarding claims 8, 17, 19, 21, and 24, Matsusaka's switching circuit includes a digital circuit (501-502; 602-603; 12-13; and logic gate 26 – see Figs. 1, 4, 6, 10, and 11, respectively).

Regarding claims 11-12, 18, & 33, Matsusaka's apparatus is a DAC (see the title) for converting a plurality of input bits (the signal 500 – Fig. 1) into an analog (current at port 505 or 506; voltage at port 509 or 510) signal, comprising: m-pieces of current sources (k x I currents); and a switching means (including 501, 502, 504s) having a plurality of input terminals (71-72s) and output terminals (75-76s), wherein the current

sources/paths are each connected to one of the different output terminals (75s or 76s based on the selection signals – SEL1 or SEL2), and the switching circuit selects an output terminal to be connected to input terminals by using input digital voltages (D0...Dn) and signals input externally (78 of Fig. 5, 77 of Fig. 7, and 79-80 of Fig. 8).

Regarding claims 13-14, 26, 28, & 34, these claims are rejected for the similar reasons as above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-4, 9-10, 18-19, 22-23, and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsusaka (US 6,498,575 B2) in view of Gu (US 6,525,683). Matsusaka discloses every aspect of the claimed invention of the above claimed except for the display/electronic apparatus as recited in the above claims. Gu discloses a display (Figs. 1A, 3B, and 5) and/or an electronic apparatus that includes the same type of semiconductor device of the claimed invention (i.e., current steering digital-to-analog convert for controlling/providing current to a display devices – see column 1, lines 49-55) (see Fig. 5). Therefore, the inclusion of the semiconductor as taught/suggested by Matsusaka in a/an display/electronic apparatus as suggested by Gu would have been obvious to one skilled person in the relevant art because it is

capable of providing a desired electrical current to a selected pixel(s) of the display device (see column 1, lines 49+).

Allowable Subject Matter

5. Claims 15, 16, 25, 27, and 29 are allowed.

Response to Remarks

6. Applicant's remarks filed 2-28-2005 have been fully considered but they are not persuasive. The applicant contents that Matsusaka does not or fails to teach the following claimed features of the independent claims: (1) the number of current sources and the number of output terminals are the same; and (2) each of the current sources connected to one of different output terminals. As disclosed by Matsusaka, each of the sub-switching circuits 504 (see Figs. 2, 5, 7, 8, and 11 – steering current cell type) is configured (by the signal 500 – Fig.1) to receive a current (is) from the (k) current sources (503 of Fig. 1) and to output the received current(s) to the output terminals (75s, 76s, 505, or 506) of the sub-switching circuits 504 (see Figs. 1-3, and 11). As seen in rows 2-3 of Fig. 3, when the values of the selection signals (SEL1 and SEL2) are not equal, each of the received current (is) from the (k) current sources is sent to the k output terminals (either the output terminals 75s or the output terminals 76 of the k sub-switching circuits 504). Therefore, the number of current sources and the numbers of output terminals used (75s or 76) are the same. Fig. 11 of Matsusaka disclosed each of the current sources (21) connected to one of the different output terminals (22 or 23). For these reasons, the above rejected claims are maintained.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 8:00 to 4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KN
March 10, 2005

Michael J. Tokar

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